CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor device comprising an N channel metal oxide semiconductor (MOS) transistor, the N channel MOS transistor including:

a P type semiconductor substrate;

~~first and second~~ an N type epitaxial ~~regions~~ region on the P type semiconductor substrate;

a first P type buried layer isolating the N ~~first and second~~ type epitaxial ~~regions~~ region from ~~each other~~ another element;

an N well in the ~~first~~ N type epitaxial region;

a drain region in the N well;

a P well surrounding ~~sides of~~ the N well and ~~isolating~~ not in physical contact with the N well;

a source region in the P well;

a gate on ~~upper layer portions of each of~~ the drain region and the source region;

a second P type buried layer between the N well and the P well and the P type semiconductor substrate, contiguous to the P well and not in physical contact with the P type semiconductor substrate and the first P type buried layer;

an N type buried layer contiguous to the second P type buried layer and the P type semiconductor substrate and not in physical contact with the P well, the N well, and the first P type buried layer; and

a first electrode electrically connected to the N type epitaxial region~~,~~ and a second electrode electrically connected to the P type semiconductor substrate~~, and a third electrode electrically connected to~~ through the first P type buried layer, the first~~,~~ and second~~, and third~~ electrodes being connected to ground potential.

2. (Currently Amended) ~~The~~ A semiconductor device ~~according to claim 1,~~ comprising an N channel metal oxide semiconductor (MOS) transistor, the N channel MOS transistor including:

a P type semiconductor substrate;

an N type epitaxial region on the P type semiconductor substrate;

a first P type buried layer isolating the N type epitaxial region from another element;

an N well in the N type epitaxial region;

a drain region in the N well;

a P well surrounding the N well and not in physical contact with the N well;

a source region in the P well;

a gate on the drain region and the source region;

a second P type buried layer between the N well and the P well and the P type semiconductor substrate, contiguous to the P well and not in physical contact with the P type semiconductor substrate and the first P type buried layer;

an N type buried layer contiguous to the second P type buried layer and the P type semiconductor substrate and not in physical contact with the P well, the N well, and the first P type buried layer;

a first electrode electrically connected to the N type epitaxial region and a second electrode electrically connected to the P type semiconductor substrate through the first P type buried layer, the second electrode being connected to ground potential; and

a connection between the first electrode and the ground potential so that a power supply potential can be supplied to the ~~first~~ N type epitaxial region.

3. (Currently Amended) The semiconductor device according to claim 1, wherein the source region is ~~a first~~ an N type semiconductor region, ~~and~~ the semiconductor device further including a ~~fourth~~ third electrode electrically connected to the source region and contacting both of the ~~first~~ N type semiconductor region, and a ~~first~~ P type semiconductor region, the P type semiconductor region surrounding the ~~first~~ N type semiconductor region ~~and spaced from~~, the third electrode not being in physical contact with the P well.

4. (Currently Amended) The semiconductor device according to claim 1, wherein the drain region is ~~a second~~ an N type semiconductor region.

5. (Currently Amended) The semiconductor device according to claim 1, wherein the first electrode is connected to ~~a third~~ an N type semiconductor region in the ~~first~~ N type epitaxial region and is not in physical contact with the N type epitaxial region.

6. (Currently Amended) The semiconductor device according to claim 1, wherein the second electrode is connected to a ~~second~~ P type semiconductor region in the first P type buried layer and is not in physical contact with the first P type buried layer.

7. (Previously Presented) The semiconductor device according to claim 1, wherein the semiconductor device is a switching element of an inverter of a motor driver.

8. (New) The semiconductor device according to claim 2, wherein the source region is an N type semiconductor region, the semiconductor device further including a third electrode electrically connected to the source region and contacting both of the N type semiconductor region and a P type semiconductor region, the P type semiconductor region surrounding the N type semiconductor region, the third electrode not being in physical contact with the P well.

9. (New) The semiconductor device according to claim 2, wherein the drain region is an N type semiconductor region.

10. (New) The semiconductor device according to claim 2, wherein the first electrode is connected to an N type semiconductor region in the N type epitaxial region and is not in physical contact with the N type epitaxial region.

11. (New) The semiconductor device according to claim 2, wherein the second electrode is connected to a P type semiconductor region in the first P type buried layer and is not in physical contact with the first P type buried layer.

12. (New) The semiconductor device according to claim 2, wherein the semiconductor device is a switching element of an inverter of a motor driver.